WHAT IS CLAIMED IS:

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1. A method of decoding encoded image data comprising the steps of:

operating a decoder circuit implemented in hardware to perform at least one non-memory intensive image decoding operation to generate, from the encoded image data, a first set of processed image data, the at least one non-memory intensive image decoding operation being an operation in the group of operations consisting of a variable length decoding operation, an inverse scan conversion operation, and an inverse quantization operation;

supplying the first set of processed image data generated by the decoder circuit to a programmable processor; and

operating the programmable processor to perform at least one additional image decoding operation using the first set of processed image data.

2. The method of claim 1, wherein the step of operating the decoder circuit, includes the step of performing at least two additional operations from the group of operations consisting of a variable length decoding operation, an inverse scan conversion operation, an inverse quantization operation, an inverse discrete cosine transform operation, and a data reduction operation, the two additional operations being different from said at least one non-memory intensive operation.

3. The method of claim 1, wherein the step of operating the decoder circuit further includes:
operating the decoder circuit to perform a data reduction operation.

4. The method of claim 2, wherein the step of operating the decoder circuit further includes:
operating the decoder circuit to perform a data reduction operation.

5. The method of claim 2, wherein the step of operating the programmable processor to perform at least one additional image decoding operation includes the step of:

operating the programmable processor to perform a motion compensated prediction operation.

6. The method of claim 5, wherein the step of operating the programmable processor to perform at least one additional image decoding operation further includes the step of:

operating the programmable processor to combine decoded image data produced by performing the motion compensated prediction operation with decoded residual image data to produce a set of decoded image data representing reconstructed pixels.

7. The method of claim 1, wherein the step of operating the programmable processor to perform at least one additional image decoding operation includes the step of:

operating the programmable processor to combine decoded image data produced by performing a motion compensated prediction operation with decoded intra-coded image data to produce a set of decoded image data representing a complete frame.

8. The method of claim 2, wherein the programmable processor is coupled to a graphics processor, the method further comprising the step of:

operating the graphics processor to perform a motion compensated prediction operation using data included in the first set of processed data.

9. The method of claim 8, wherein the step of operating the programmable processor to perform at least one additional image decoding operation further includes the step of:

operating the programmable processor to combine decoded image data produced by performing the motion compensated prediction operation with decoded residual image data to produce a set of decoded image data representing reconstructed pixels.

10. The method of claim 8, further comprising the step of:

storing in the decoder circuit multiple sets of context information, each set of stored context information corresponding to a different one of a plurality of encoded data streams processed by the decoder circuit.

11. The method of claim 1, further comprising the step of:

storing in the decoder circuit multiple sets of context information, each set of stored context information corresponding to a different one of a plurality of encoded data streams processed by the decoder circuit.

12. The method of claim 11, further comprising the step of:

operating the decoder circuit to access the stored set of context information corresponding to an encoded data stream when the data stream is to be processed by the decoder circuit.

13. The method of claim 12, wherein each set of stored context information includes encoded data stream syntax information.

14. A method of decoding encoded image data including inter-coded image data and intra-coded image data, the method comprising the steps of:

operating an intra-coded video decoder circuit implemented in hardware to decode said intra-coded image data and to output prediction residual data produced from said encoded image data; and

controlling a programmable processor to perform an inter-coded decoding operation using said prediction residual image data.

15. The decoding method of claim 14, wherein the step of controlling a programmable processor to perform a decoding operation includes the step of:

controlling the programmable processor to perform a motion compensated prediction operation.

16. The decoding method of claim 14, wherein the step of controlling a programmable processor to perform an inter-coded decoding operation includes the step of:

operating the programmable processor to control the supply of motion vector information to a graphics processor.

17. The decoding method of claim 14, further comprising the step of:

controlling a graphics processor coupled to said programmable processor to perform a motion compensated prediction operation.

18. The decoding method of claim 14, wherein the step of operating the decoder circuit to decode said intra-coded image data includes performing a complete decoding operation on said intra-coded image data to produce fully decoded image data therefrom.

19. A method of decoding encoded image data comprising the steps of:

operating a decoder circuit implemented in hardware to perform non-memory intensive image decoding operations to generate, from the encoded image data, a first set of processed image data, at least one of said non-memory intensive image decoding operation being a data reduction operation;

supplying the first set of processed image data generated by the decoder circuit to a programmable processor; and

operating the programmable processor to perform at least one additional image decoding operation using the first set of processed image data.

20. A system for decoding encoded image data including intra-coded image data and inter-coded image data, the system comprising:

an intra-coded data decoding circuit for decoding intra-coded image data;

a programmable processor coupled to the intra-coded data decoding circuit; and

a memory including a video decoding routine for controlling the programmable processor to perform at least one inter-coded data decoding operation.

21. The system of claim 20, further comprising:

a graphics processor coupled to the programmable processor.

22. The system of claim 20, wherein the intra-coded data decoding circuit includes:

an inverse discrete cosine transform circuit and an inverse quantization circuit.

23. The system of claim 22, further comprising:

a motion vector reconstruction circuit for reconstructing motion vectors included in said inter-coded image data, the motion vector reconstruction circuit being coupled to said programmable processor.

24. The system of claim 23, wherein said intra-coded data decoding circuit and motion vector reconstruction circuit are implemented on a first semiconductor chip and wherein said programmable processor is implemented on a second semiconductor chip.

25. The system of claim 23, wherein said intra-coded data decoding circuit, motion vector reconstruction circuit and programmable processor are implemented on a single semi-conductor chip.

26. The system of claim 20, wherein the intra-coded data decoding circuit includes a variable length decoding circuit for processing both intra-coded and inter-coded image data.

27. The system of claim 26,

wherein the intra-coded data decoding circuit further includes an inverse discrete cosine transform circuit and an inverse quantization circuit;

wherein the system further includes a motion vector reconstruction circuit for reconstructing motion vectors included in said inter-coded image data coupled to said programmable processor; and

wherein the variable length decoding circuit includes means for outputting intra-coded data to the inverse quantization circuit and means for outputting motion vector information to the motion vector reconstruction circuit.

28. The system of claim 20, wherein the intra-coded data decoding circuit and the programmable processor are implemented on two separate semi-conductor chips.

29. An apparatus for processing encoded image data including motion vector information, the apparatus comprising:

a motion vector reconstruction circuit for performing motion vector reconstruction operations using motion vector information included in the encoded image data; and

means for outputting to a programmable processor reconstructed motion vectors generated by the motion vector reconstruction circuit.

30. The apparatus of claim 29, further comprising:

said programmable processor coupled to the means for outputting; and

a memory device coupled to said programmable processor, the memory device including a video decoding routine used to control said programmable processor to perform a video decoding operation using reconstructed motion vectors received from the means for outputting.